



Data Sheet

NT96650-ES

Hybrid DSC/DV Processor

Version 0.3

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Revision History

| Rev. | Date | Author | Contents |
|------|------------|------------|---|
| 0.1 | 2012/02/13 | Kevin Hung | First draft version. |
| 0.2 | 2012/03/16 | Kevin Hung | For PM |
| 0.3 | 2012/09/07 | Kevin Hung | Add pin number & DDR_PHY(DLL) power issue |
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| | | | |
| | | | |

| Type | Issue | Solution |
|----------------------------|--------------------------------------|-----------------------------|
| Function(interior of chip) | MPLL start-up time | BE solution & ROM code flow |
| Power | DDR_PHY(DLL) voltage of power supply | Two kinds of version |
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Features

■ High Performance 32-bit CPU

- MIPS32 24Kec with ASE DSP extension
- MMU embedded
- 16KB instruction and 16KB data cache
- Embedded ICE makes firmware debugging easier
- CPU operating frequency up to 480MHz, on the fly programmable

■ Power Management features

- Firmware configurable operating frequency of each functional block to meet best power budget
- Internal power domain partition

■ Integrated Clock Generator

- Internal PLL with spread spectrum capability
- 12MHz system/USB oscillator
- 32768Hz RTC oscillator

■ Scalable Memory Bus Architecture

- 16-bit DDR2 / DDR3 SDRAM bus, supporting up to 2Gb DDR SDRAM
- DRAM operating frequency up to 400MHz without ODT
- Tunable DDR frequency on the fly for power saving

■ Sensor Interface Engine

- Support up to 50M pixels CCD/CMOS image sensor
- Support high speed serial interface like sub-LVDS/Mipi/HiSPi up to 10 channels for most commercial CMOS sensors including Sony, Panasonic, Aptina, Samsung, Sharp and Omnivision, etc.
- Support parallel sensor interface for most commercial CCD sensors including Sony, Panasonic, Sharp and CMOS sensors including Aptina and Omnivision
- Support BT.601/656 video input
- Support dual sensors input (dual Mipi version only)
- Support 12-bit (serial) sensor data input
- Support high speed serial interface sensor pixel rate up to 576MPixels/sec
- Support continuous shot up to 10 fps for 16MP sensor
- Support parallel interface sensor pixel clock up to 108MHz
- Support movie CCD, and horizontal division CCD of SONY
- Support multiple field, line interleaved CCD of Sharp

- Support smear reduction for CCD sensor
- Built-in color pattern generation
- Sensor black level clamping
- Efficient defect concealment algorithm
- Raw image sub-sample for video & high ISO image
- Flexible image analysis flow for AE, AWB and AF purpose
- Programmable histogram analysis
- Automatic flicker detection
- R/G/B Gamma LUT for sensor linearization correction
- In-pipeline lens shading compensation technology
- In-pipeline color shading compensation technology
- In-pipeline geometric distortion correction technology
- In-pipeline color aberration correction technology
- Support CMOS sensor spatial crosstalk cancellation
- Support in-frame dark frame subtraction with smart defect detection algorithm
- Support rolling shutter correction for CMOS sensor
- Mechanical shutter control
- Flash light control

■ Image Processing Engine

- Proprietary advanced anti-alias Bayer CFA color interpolation
- Flexible edge rendering, control and enhancement
- Powerful noise reduction technology for still and video recording
- Support motion compensated temporal filtering (MCTF) for efficient video noise reduction
- Support temporal noise reduction with ghost reduction
- R/G/B Gamma LUT
- High precision color correction matrix for sRGB or specific color requirement
- Brightness/contrast and hue/saturation adjustment
- Specific color control technology (Patent)
- 3D color conversion for specific color preference tuning
- False color suppression
- Support wide dynamic range (WDR) for local illumination enhancement

■ Image Manipulation Engine

- High quality scaling engine for seamless digital zooming from 1/16x to 16x
- Support thumbnail image generation

- Forward/inverse color space transform

■ Face Detection Engine

- Very high speed face detection and tracking
- High accuracy under different light source
- Programmable target data base

■ Digital Image Stabilizer

- Remove unintended hand movement from an image sequence
- Single frame compensation for video (Total compensation)
- Accumulate frame compensation for video (Smart compensation)
- Motion refresh rate 60Hz
- Interface search range up to ± 32
- Programmable total compensation range
- Accommodate resolution 1080p
- Adjustable number of motion vectors for motion estimation. Maximum 1024 motion vectors per process (16 regions x 64 blocks/region).

■ LCD/TV Display

- Support dual display including LCD panel and HDMI/TV display simultaneously
- High performance scaling up/down engine, programmable gamma correction, color transform and color management for LCD or TV display
- Separate OSD for LCD panel and TV
- Support digital LCD interface for AUO, Casio, CMI (all digital panels will be supported)
- Support 16-bit RGB parallel interface (RGB565 or Delta RGB) LCD panel up to 1024x1024 resolution
- Support MIPI DSI for mobile display
- Support 90° rotation/flip/mirror
- Support PAL / NTSC video encoder (CVBS format)
- Integrated 1 internal 10-bit video DACs
- Support digital interface BT.601/656/1120 output port
- 3.3V / 1.8V LCD / Digital video out

■ HDMI

- Support HDMI v1.3a
- Support DDC with maximum 100kHz access rate for CEA-861-D format
- Support CEC
- Support 16 bits PCM 32 KHz, 44.1 KHz, 48KHz for maximum 2 channels audio output

■ Graphic Engine

- Copy and paste
- Geometric operation including mirror, flip and rotation
- Arithmetic operation including addition, subtraction, color keying, logic operation and alpha blending
- Support warping function
- Support anti-alias affine transform
- Support hardware acceleration for multi-frame processing

■ Cipher

- 64-bit DES, 3DES, and AES-128
- Both encryption and decryption
- Big and little endian of input data

■ H.264/AVC CODEC

- Support encoder BP/MP, level 4.1
- Support encoder HP, level 4.2
- Support real-time capability for 1080p30, 720p60, 480p120
- Support full frame still capture while video recording
- H.264 high/main profile
- 1 reference picture for P-frame, 2 reference pictures for B-frame
- Support video format MP4, AVI, MOV
- Support bit rate control
- Automatic frame sync for high frame rate

■ Motion Estimation

- [-124.75,+124.75] search range in horizontal component
- [-28.75, +28.75] search range in vertical component
- MB mode: 16x16, 16x8, 8x16, 8x8, skip, and direct (B-frame)

■ F/W Audio CODEC

- AAC encode / decode (32KHz, 48KHz @ 192kbps)
- ADPCM encode / decode
- Noise cancellation for background noise, motor operation, and wind

■ H/W Audio CODEC

- stereo 16-bits ADC audio recording
- stereo 16-bits DAC audio playback
- Programmable ALC / Noise Gate I

- Audio sampling rate : 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48kHz
- Support dual microphone inputs
- On-chip speaker driver / stereo headphone drive

■ JPEG CODEC

- Supports Motion JPEG 30fps@1080P30 video clip/playback function
- Max. pixel clock 120Mpixel / sec
- Support ISO/IEC 10918-1 baseline JPEG compression/decompression.
- Still image maximum resolutions will be up to 65536x65536 pixels
- Support input format: 422, 420, 411, 400, 211
- JPEG supports downloadable Quantization and Huffman tables
- Support Exchangeable Image File format (EXIF 2.2.3 and newer)
- Support MPO file format for 3D image

■ Digital Audio Interface

- Support I2S codec interface
- Audio clock generator

■ Dual Graphic-based OSD

- Support 8-bit palette and ARGB(4565 or 8565) OSD architecture
- 256 colors simultaneously out of true color at 8-bit palette OSD
- 8 levels of opacity for 8-bit palette OSD
- Programmable width & height to meet LCD/TV's resolution exactly
- Picture in picture function
- Dedicated 16 face frames for face detection function

■ Storage Memory Controller

- Secure Digital card and SDIO
- Support SD 3.0
- Support UHS-I: UHS50, UHS104 (Max. freq. 108MHz)
- Support eMMC and hot boot
- Support eyeFi for wireless connection
- Multi-Media card
- SLC NAND type flash

■ USB

- Fully compliant with USB2.0 device/host
- High speed (480Mbps) supported
- Optionally switchable to be fully compliant with USB 1.1

- Support Control / Isochronous / Interrupt and Bulk transfer
- Support PC camera mode

■ **Timers**

- RTC can be powered by separate backup battery and operating from 1.5V to 3.6V
- Watch dog timer
- 16 programmable HW timers support resolution up to 3MHz and 32 bits counter

■ **Peripheral Interface**

- Support I2C interface
- Support 20 channels PWM including built-in 16 (4 sets) pattern generators for μ -Stepping motor control.
- Support GPIO and flexible PWM interface with micro-stepping
- Support programmable 3-wired serial interface
- Support SPI for gyroscope reading
- Support UART interface
- Support 8 channels of 10-bit ADC with touch panel interface (2 channels), the max. sample rate up to 12.5 KHz per channel

■ **On-chip Boot Strap Loader**

- Built-in on-chip mask ROM
- User program can be stored in NAND-type flash and external static memory is not necessary
- On-chip mask ROM can be disabled
- System can boot from SPI flash, NAND flash, memory cards, eMMC and USB

■ **Triple Voltage Power Supply**

- 1.0V core logic voltage
- 1.8V / 1.5V DDRII/DDRIII SDRAM interface voltage
- 3.3V I/O interface and analog circuit voltage

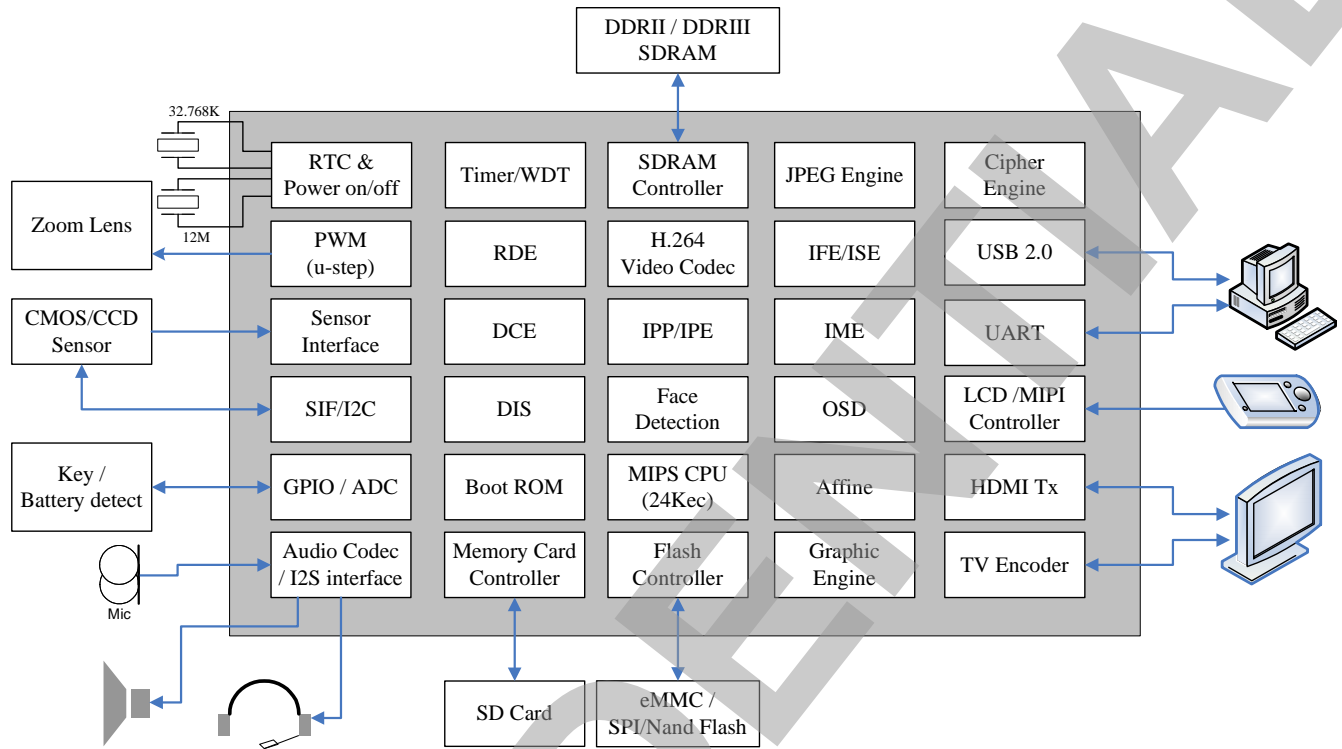
■ **Package**

- NT96650BG: 305 ball TFBGA, 13x13 mm²

General Description

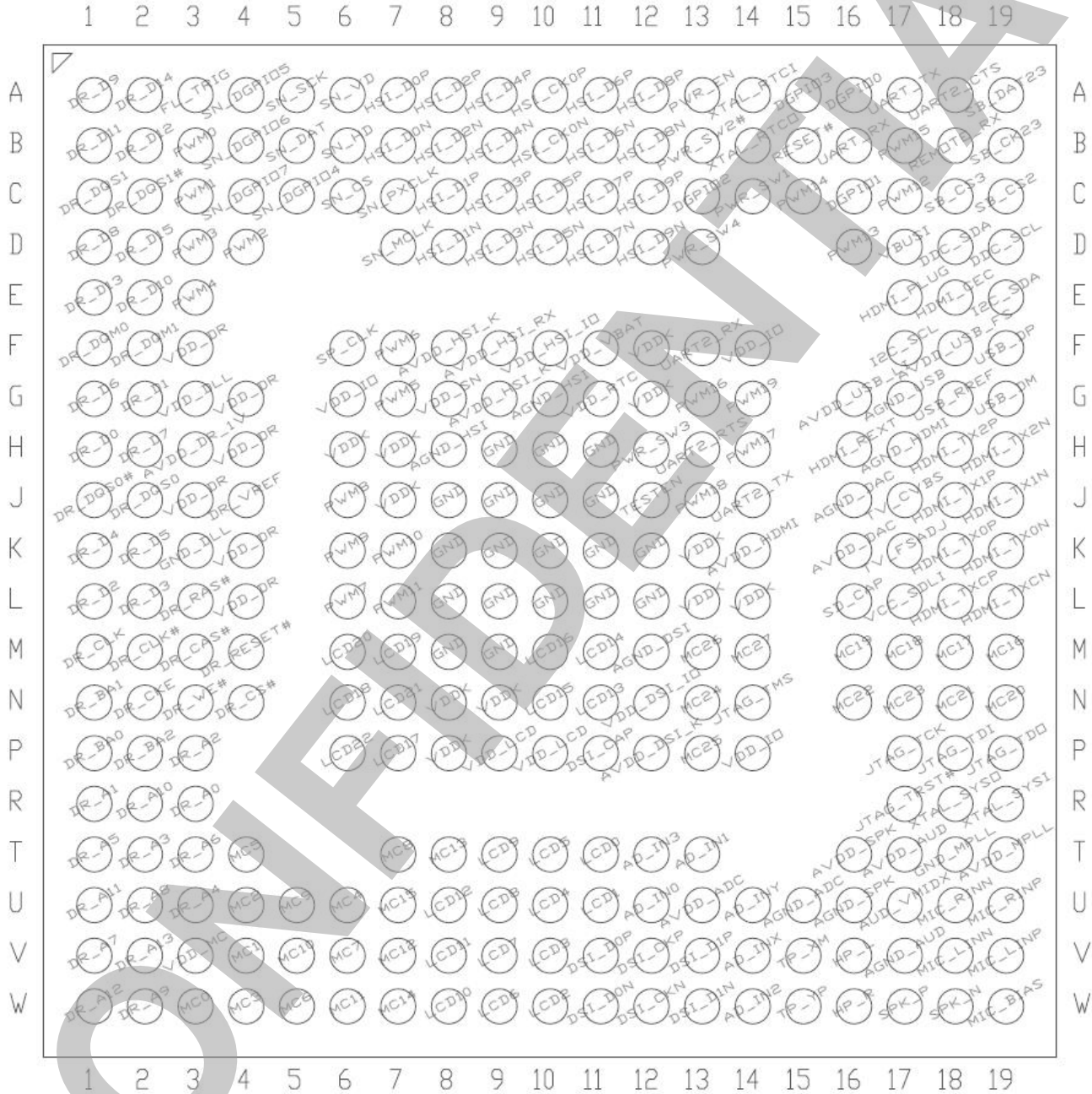
NT96650BG is a high image quality, high performance, power saving and cost effective digital still camera (DSC) and digital video camera (DV) controller with excellent digital still image capturing and video streaming capabilities. It is targeted for the application of VGA to 50M pixel DSC/DV resolutions. It can be easily adapted to many high speed CMOS and conventional CCD image sensors with on chip programmable interface timing approach. The controller provides sophisticated video processing methods with built-in hardware acceleration pipeline. This is essential for achieving high performance for per-shot, shot-to-shot, and continuous shooting pictures. The controller provides flexible mechanism for auto white balance, auto exposure and auto-focusing in order to better tradeoff hardware and software efforts over the performance. Embedded H.264 video CODEC supports video recording up to full-HD 1080p30. The HDMI 1.3 Tx is also equipped for HDTV output. Rich storage interfaces are supported to make it ideal for the storage of still pictures and video streaming data. The USB2.0 high speed interface can upload/download the audio/video data efficiently to/from PC.

Block Diagram



Pin Configuration

TFBGA-305



| Pin No | Pin Name | Pin No | Pin Name | Pin No | Pin Name | Pin No | Pin Name |
|--------|------------|--------|-------------|--------|------------|--------|------------|
| A1 | DR_D9 | E19 | I2C_SDA | K11 | GND | R3 | DR_A0 |
| A2 | DR_D14 | F1 | DR_DQM0 | K12 | GND | R17 | JTAG_TRST# |
| A3 | FL_TRIG | F2 | DR_DQM1 | K13 | VDDK | R18 | XTAL_SYSO |
| A4 | SN_DGPIO5 | F3 | VDD_DR | K14 | AVDD_HDMI | R19 | XTAL_SYSI |
| A5 | SN_SCK | F6 | SP_CLK | K16 | AVDD_DAC | T1 | DR_A5 |
| A6 | SN_VD | F7 | PWM6 | K17 | TV_FSADJ | T2 | DR_A3 |
| A7 | HSI_D0P | F8 | AVDD_HSI_K | K18 | HDMI_TX0P | T3 | DR_A6 |
| A8 | HSI_D2P | F9 | AVDD_HSI_RX | K19 | HDMI_TX0N | T4 | MC5 |
| A9 | HSI_D4P | F10 | VDD_HSI_IO | L1 | DR_D2 | T7 | MC8 |
| A10 | HSI_CK0P | F11 | VDD_VBAT | L2 | DR_D3 | T8 | MC13 |
| A11 | HSI_D6P | F12 | VDDK | L3 | DR_RAS# | T9 | LCD9 |
| A12 | HSI_D8P | F13 | UART2_RX | L4 | VDD_DR | T10 | LCD5 |
| A13 | PWR_EN | F14 | VDD_IO | L6 | PWM7 | T11 | LCD0 |
| A14 | XTAL_RTCI | F17 | I2C_SCL | L7 | PWM11 | T12 | AD_IN3 |
| A15 | DGPIO3 | F18 | AVDD_USB_FS | L8 | GND | T13 | AD_IN1 |
| A16 | DGPIO0 | F19 | USB_DP | L9 | GND | T16 | AVDD_SPK |
| A17 | UART_TX | G1 | DR_D6 | L10 | GND | T17 | AVDD_AUD |
| A18 | UART2_CTS | G2 | DR_D1 | L11 | GND | T18 | GND_MPLL |
| A19 | SB_DAT23 | G3 | AVDD_DLL | L12 | GND | T19 | AVDD_MPLL |
| B1 | DR_D11 | G4 | VDD_DR | L13 | VDDK | U1 | DR_A11 |
| B2 | DR_D12 | G6 | VDD_IO | L14 | VDDK | U2 | DR_A8 |
| B3 | PWM0 | G7 | PWM5 | L16 | SD_CAP | U3 | DR_A4 |
| B4 | SN_DGPIO6 | G8 | VDD_SN | L17 | VDD_SDLI | U4 | MC2 |
| B5 | SN_DAT | G9 | AVDD_HSI_K | L18 | HDMI_TXCP | U5 | MC9 |
| B6 | SN_HD | G10 | AGND_HSI | L19 | HDMI_TXCN | U6 | MC4 |
| B7 | HSI_D0N | G11 | VDD_RTC | M1 | DR_CLK | U7 | MC15 |
| B8 | HSI_D2N | G12 | VDDK | M2 | DR_CLK# | U8 | LCD12 |
| B9 | HSI_D4N | G13 | PWM16 | M3 | DR_CAS# | U9 | LCD8 |
| B10 | HSI_CK0N | G14 | PWM19 | M4 | DR_RESET# | U10 | LCD4 |
| B11 | HSI_D6N | G16 | AVDD_USB_LI | M6 | LCD20 | U11 | LCD1 |
| B12 | HSI_D8N | G17 | AGND_USB | M7 | LCD19 | U12 | AD_IN0 |
| B13 | PWR_SW2# | G18 | USB_RREF | M8 | GND | U13 | AVDD_ADC |
| B14 | XTAL_RTICO | G19 | USB_DM | M9 | GND | U14 | AD_INY |
| B15 | RESET# | H1 | DR_D0 | M10 | LCD16 | U15 | AGND_ADC |
| B16 | UART_RX | H2 | DR_D7 | M11 | LCD14 | U16 | AGND_SPK |
| B17 | PWM15 | H3 | AVDD_DR_1V | M12 | AGND_DSI | U17 | AUD_VMDX |
| B18 | REMOTE_RX | H4 | VDD_DR | M13 | MC26 | U18 | MIC_RINN |
| B19 | SB_CK23 | H6 | VDDK | M14 | MC27 | U19 | MIC_RINP |
| C1 | DR_DQS1 | H7 | VDDK | M16 | MC19 | V1 | DR_A7 |
| C2 | DR_DQS1# | H8 | AGND_HSI | M17 | MC18 | V2 | DR_A13 |
| C3 | PWM1 | H9 | GND | M18 | MC17 | V3 | VDD_MC |
| C4 | SN_DGPIO7 | H10 | GND | M19 | MC16 | V4 | MC1 |
| C5 | SN_DGPIO4 | H11 | GND | N1 | DR_BA1 | V5 | MC10 |
| C6 | SN_CS | H12 | PWR_SW3 | N2 | DR_CKE | V6 | MC7 |
| C7 | SN_PXCLK | H13 | UART2_RTS | N3 | DR_WE# | V7 | MC12 |
| C8 | HSI_D1P | H14 | PWM17 | N4 | DR_CS# | V8 | LCD11 |
| C9 | HSI_D3P | H16 | HDMI_REXT | N6 | LCD18 | V9 | LCD7 |
| C10 | HSI_D5P | H17 | AGND_HDMI | N7 | LCD21 | V10 | LCD3 |
| C11 | HSI_D7P | H18 | HDMI_TX2P | N8 | VDDK | V11 | DSI_D0P |
| C12 | HSI_D9P | H19 | HDMI_TX2N | N9 | VDDK | V12 | DSI_CKP |
| C13 | DGPIO2 | J1 | DR_DQS0# | N10 | LCD15 | V13 | DSI_D1P |
| C14 | PWR_SW1 | J2 | DR_DQS0 | N11 | LCD13 | V14 | AD_INX |
| C15 | PWM14 | J3 | VDD_DR | N12 | VDD_DSI_IO | V15 | TP_XM |
| C16 | DGPIO1 | J4 | DR_VREF | N13 | MC24 | V16 | HP_L |
| C17 | PWM12 | J6 | PWM8 | N14 | JTAG_TMS | V17 | AGND_AUD |
| C18 | SB_CS3 | J7 | VDDK | N16 | MC22 | V18 | MIC_LINN |
| C19 | SB_CS2 | J8 | GND | N17 | MC23 | V19 | MIC_LINP |
| D1 | DR_D8 | J9 | GND | N18 | MC21 | W1 | DR_A12 |
| D2 | DR_D15 | J10 | GND | N19 | MC20 | W2 | DR_A9 |

| | | | | | | | |
|-----|-----------|-----|-----------|-----|------------|-----|----------|
| D3 | PWM3 | J11 | GND | P1 | DR_BA0 | W3 | MC0 |
| D4 | PWM2 | J12 | TESTEN | P2 | DR_BA2 | W4 | MC3 |
| D7 | SN_MCLK | J13 | PWM18 | P3 | DR_A2 | W5 | MC6 |
| D8 | HSI_D1N | J14 | UART2_TX | P6 | LCD22 | W6 | MC11 |
| D9 | HSI_D3N | J16 | AGND_DAC | P7 | LCD17 | W7 | MC14 |
| D10 | HSI_D5N | J17 | TV_CVBS | P8 | VDDK | W8 | LCD10 |
| D11 | HSI_D7N | J18 | HDMI_TX1P | P9 | VDD_LCD | W9 | LCD6 |
| D12 | HSI_D9N | J19 | HDMI_TX1N | P10 | VDD_LCD | W10 | LCD2 |
| D13 | PWR_SW4 | K1 | DR_D4 | P11 | DSI_CAP | W11 | DSI_D0N |
| D16 | PWM13 | K2 | DR_D5 | P12 | AVDD_DSI_K | W12 | DSI_CKN |
| D17 | VBUSI | K3 | AGND_DLL | P13 | MC25 | W13 | DSI_D1N |
| D18 | DDC_SDA | K4 | VDD_DR | P14 | VDD_IO | W14 | AD_IN2 |
| D19 | DDC_SCL | K6 | PWM9 | P17 | JTAG_TCK | W15 | TP_YP |
| E1 | DR_D13 | K7 | PWM10 | P18 | JTAG_TDI | W16 | HP_R |
| E2 | DR_D10 | K8 | GND | P19 | JTAG_TDO | W17 | SPK_P |
| E3 | PWM4 | K9 | GND | R1 | DR_A1 | W18 | SPK_N |
| E17 | HDMI_PLUG | K10 | GND | R2 | DR_A10 | W19 | MIC_BIAS |
| E18 | HDMI_CEC | | | | | | |

Pin Descriptions

I = input port with Schmitt trigger

O = output port with normal driving/sinking

I/O = bi-directional port with normal driving/sinking and Schmitt input

mvI/O = multi voltage bi-direction port with Schmitt input

HSI = high speed serial interface with multi voltage input port

I/Osw = bi-directional port with strong driving/sinking and wide Schmitt input range

I/Ow = bi-directional port with wide Schmitt input range

I/Os = bi-directional port with strong driving/sinking

I/Oss = bi-directional port with strong driving/sinking

I/Oz = bi-directional port with large pull/down resistor

I/O_{5VT} = bi-directional port with normal driving/sinking and Schmitt input

OD = open drain output with normal sinking

I/OD = bi-directional port, open drain output

LVD = low voltage detect function pin

p/u = internal pull-up

p/d = internal pull-down

AI = analog input port

AI_{5VT} = analog 5V tolerant input port

AO = analog output port

AI/O = analog bi-directional port

H = output high

L = output low

P = power or ground

Note: * means this pin has interrupted function.

NT96650BG 305 pins

Total: 144 pins

Alternative GPIO: 44 total pins

System interface (9)

| Pin No. | Name | Type | Reset | Descriptions |
|---------|---------------------------|------|-------|---|
| R19 | XTAL_SYSI | AI | - | Crystal input for system oscillator. (12MHz) |
| R18 | XTAL_SYSO | AO | - | Output for system oscillator. |
| B15 | RESET# | LVD | p/u | System Reset. Connect a capacitor to ground for reset time control. |
| J12 | TESTEN | I | I p/d | Test mode enable. Keep low for normal operation. |
| R17 | JTAG_TRST# P_GPIO[31]* | IO | I p/u | JTAG test logic reset(active low). |
| N14 | JTAG_TMS P_GPIO[32]* | IO | I p/d | JTAG test mode select. |
| P17 | JTAG_TCK P_GPIO[33]* | IO | I p/d | JTAG test clock input. |
| P18 | JTAG_TDI P_GPIO[34]* | IO | I p/d | JTAG test data input. |
| P19 | JTAG_TDO P_GPIO[35]* | IO | I p/d | JTAG test data output. |

RTC & Power Button Controller (7)

| Pin No. | Name | Type | Default | Descriptions |
|---------|-----------|-------------------|---------|---|
| A14 | XTAL_RTCI | AI | - | Crystal input for real time clock oscillator. (32.768KHz). |
| B14 | XTAL_RTCO | AO | - | Output for real time clock oscillator. |
| C14 | PWR_SW1* | AI | I p/d | Power on/off signal input. (ON/OFF switch use) |
| B13 | PWR_SW2*# | AI | I p/u | Power on/off signal input. (falling edge trigger) |
| H12 | PWR_SW3 | I _{5VTZ} | I p/d | Power on/off signal input. (5V tolerance Input for VBUSI use) |
| D13 | PWR_SW4 | AI | I p/d | Power on/off signal input. (Bettery in use) |
| A13 | PWR_EN | AO | - | Power enable signal output. |

* PWR_SW can trigger interrupt (share RTC interrupt). If this pin isn't used, Novatek recommends connecting this pin to GND.

DRAM interface (48)

| Pin No. | Name | Type | Reset | Descriptions |
|---------|-----------|------|-------|------------------------------------|
| M4 | DR_RESET# | O | - | Reset signal output for DDR3 DRAM. |
| M1 | DR_CLK | O | - | DRAM differential clock output. |
| M2 | DR_CLK# | O | - | |
| N2 | DR_CKE | O | - | DRAM clock enable. |
| N4 | DR_CS# | O | - | DRAM control signals |
| M3 | DR_CAS# | | | |

| | | | | |
|----|----------|-----|---|---|
| L3 | DR_RAS# | | | |
| N3 | DR_WE# | | | |
| J4 | DR_VREF | AI | - | DRAM reference voltage input. |
| P1 | DR_BA0 | O | - | DRAM bank select. |
| N1 | DR_BA1 | | | |
| P2 | DR_BA2 | | | |
| R3 | DR_A0 | O | - | DRAM address bus. |
| R1 | DR_A1 | | | |
| P3 | DR_A2 | | | |
| T2 | DR_A3 | | | |
| U3 | DR_A4 | | | |
| T1 | DR_A5 | | | |
| T3 | DR_A6 | | | |
| V1 | DR_A7 | | | |
| U2 | DR_A8 | | | |
| W2 | DR_A9 | | | |
| R2 | DR_A10 | | | |
| U1 | DR_A11 | | | |
| W1 | DR_A12 | | | |
| V2 | DR_A13 | | | |
| F1 | DR_DQM0 | O | - | DRAM data mask: DQM0 corresponds to DQ0-DQ7 and DQM1 corresponds to DQ8-DQ15. |
| F2 | DR_DQM1 | | | |
| J2 | DR_DQS0 | I/O | - | DRAM data strobe. DQS0 corresponds to DQ0-DQ7 and DQS1 corresponds to DQ8-DQ15. |
| J1 | DR_DQS0# | | | |
| C1 | DR_DQS1 | | | |
| C2 | DR_DQS1# | | | |
| H1 | DR_D0 | I/O | - | DRAM data bus input/output, lower byte. (Each bits of lower byte may be permuted to make routing simpler). |
| G2 | DR_D1 | | | |
| L1 | DR_D2 | | | |
| L2 | DR_D3 | | | |
| K1 | DR_D4 | | | |
| K2 | DR_D5 | | | |
| G1 | DR_D6 | | | |
| H2 | DR_D7 | | | |
| D1 | DR_D8 | I/O | - | DRAM data bus input/output, upper byte. (Each bits of upper byte may be permuted to make routing simpler) |
| A1 | DR_D9 | | | |
| E2 | DR_D10 | | | |
| B1 | DR_D11 | | | |
| B2 | DR_D12 | | | |
| E1 | DR_D13 | | | |
| A2 | DR_D14 | | | |
| D2 | DR_D15 | | | |

Sensor interface (33)

| Pin No. | Name | Type | Reset | Descriptions |
|---------|---------|------|-------|---|
| B7 | HSI_D0N | HSI | I p/d | High speed differential sensor interface and parallel |

| | | | | | |
|-----|------------------------|---|--------|--|--------------------------------------|
| | S_GPI[0] | | | | |
| A7 | HSI_D0P S_GPI[1] | / | | | |
| D8 | HSI_D1N S_GPI[2] | / | | | |
| C8 | HSI_D1P S_GPI[3] | / | | | |
| B8 | HSI_D2N S_GPI[4] | / | | | |
| A8 | HSI_D2P S_GPI[5] | / | | | |
| D9 | HSI_D3N S_GPI[6] | / | | | |
| C9 | HSI_D3P S_GPI[7] | / | | | |
| B9 | HSI_D4N S_GPI[8] | / | | | |
| A9 | HSI_D4P S_GPI[9] | / | | | |
| B10 | HSI_CK0N S_GPI[10] | / | | interface. (when sensor interface is configured as high speed differential sensor interface, the clock lane should be a dedicated differential lane. And each data lanes may be permuted in established group, refer to below table) | |
| A10 | HSI_CK0P S_GPI[11] | / | | | |
| D10 | HSI_D5N S_GPI[12] | / | | | |
| C10 | HSI_D5P S_GPI[13] | / | | | |
| B11 | HSI_D6N S_GPI[14] | / | | | |
| A11 | HSI_D6P S_GPI[15] | / | | | |
| D11 | HSI_D7N S_GPI[16] | / | | | |
| C11 | HSI_D7P S_GPI[17] | / | | | |
| B12 | HSI_D8N S_GPI[18] | / | | | |
| A12 | HSI_D8P S_GPI[19] | / | | | |
| D12 | HSI_D9N S_GPI[20] | / | | | |
| C12 | HSI_D9P S_GPI[21] | / | | | |
| D7 | SN_MCLK S_GPIO[24] | / | mvl/Os | I p/d | Programmable Clock output for sensor |
| C7 | SN_PXCLK S_GPIO[25] | / | mvl/Os | I p/d | Sensor Pixel Clock Input |
| A6 | SN_VD | / | mvl/O | I p/d | Sensor Vertical Sync input / output |

| | | | | | |
|----|---|---|-------|-------|--|
| | S_GPIO[26] | | | | |
| B6 | SN_HD S_GPIO[27] | / | mvI/O | I p/d | Sensor Horizontal Sync input / output |
| C6 | SN_CS SPI3_CS P_GPIO[56] | / | mvIOs | I p/u | General serial interface 0 or Serial Peripheral Interface 3 Chip Select |
| A5 | SN_SCK SPI3_CLK I2C_SCL P_GPIO[57] | / | mvIOD | I p/u | General serial interface 0 or Serial Peripheral Interface 3 clock output. I2C-BUS clock output(Open Drain IO structure) |
| B5 | SN_DAT SPI3_DO I2C_SDA P_GPIO[58] | / | mvIOD | I p/u | General serial interface 0 or Serial Peripheral Interface 3 data output. I2C-BUS data input / output(Open Drain IO structure) |
| C5 | SN_DGPIO4* | | mvIO | I p/d | General purpose Input / output |
| A4 | SN_DGPIO5* | | mvIO | I p/d | General purpose Input / output |
| B4 | SPI3_DI SN_SHUTTER / SN_DGPIO6* | / | mvIO | I p/d | Serial Peripheral Interface 3 data input. Shutter signal input from sensor |
| C4 | SN_FLASH SN_DGPIO7* | / | mvIO | I p/d | Flash Signal input from sensor |

Note*: The pin can trigger interrupt.

Note1 : The input voltage of HSI corresponds to GVDD_SN.

Note2 : The mvI/O voltage of Sensor interface corresponds to VDD_SN.

| Name | LVDS | HiSPi | MIPI CSI | Parallel (12 bits) | CCIR601 (16 bits) | CCIR601 (8 bits) | |
|-----------|-----------------|-----------------|------------------|--------------------|-------------------|------------------|---|
| S_GPI[0] | HSI_D0N | SLVS_D0N | I CSI_D0N | I SN_D0 | I | | |
| S_GPI[1] | HSI_D0P | SLVS_D0P | I CSI_D0P | I SN_D1 | I | | |
| S_GPI[2] | HSI_D1N | SLVS_D1N | I CSI_D1N | I SN_D2 | I | | |
| S_GPI[3] | HSI_D1P | SLVS_D1P | I CSI_D1P | I SN_D3 | I | | |
| S_GPI[4] | HSI_D2N | SLVS_D2N | I CSI_D2N | I SN_D4 | I CCIR_Y0 | I | |
| S_GPI[5] | HSI_D2P | SLVS_D2P | I CSI_D2P | I SN_D5 | I CCIR_Y1 | I | |
| S_GPI[6] | HSI_D3N | SLVS_D3N | I CSI_D3N | I SN_D6 | I CCIR_Y2 | I | |
| S_GPI[7] | HSI_D3P | SLVS_D3P | I CSI_D3P | I SN_D7 | I CCIR_Y3 | I | |
| S_GPI[8] | HSI_D4N | | | SN_D8 | I CCIR_Y4 | I | |
| S_GPI[9] | HSI_D4P | | | SN_D9 | I CCIR_Y5 | I | |
| S_GPI[10] | HSI_CK0N | SLVS_CKN | I CSI_CKN | I SN_D10 | I CCIR_Y6 | I | |
| S_GPI[11] | HSI_CK0P | SLVS_CKP | I CSI_CKP | I SN_D11 | I CCIR_Y7 | I | |
| S_GPI[12] | HSI_D5N | | | | CCIR_C0 | I CCIR_YC0 | I |
| S_GPI[13] | HSI_D5P | | | | CCIR_C1 | I CCIR_YC1 | I |
| S_GPI[14] | HSI_D6N | | | | CCIR_C2 | I CCIR_YC2 | I |
| S_GPI[15] | HSI_D6P | | | | CCIR_C3 | I CCIR_YC3 | I |
| S_GPI[16] | HSI_D7N | | | | CCIR_C4 | I CCIR_YC4 | I |
| S_GPI[17] | HSI_D7P | | | | CCIR_C5 | I CCIR_YC5 | I |
| S_GPI[18] | HSI_D8N | | | | CCIR_C6 | I CCIR_YC6 | I |
| S_GPI[19] | HSI_D8P | | | | CCIR_C7 | I CCIR_YC7 | I |
| S_GPI[20] | HSI_D9N | | | | CCIR_VD | I CCIR_VD | I |
| S_GPI[21] | HSI_D9P | | | | CCIR_HD | I CCIR_HD | I |
| S_GPI[24] | SN_MCLK | SN_MCLK | O SN_MCLK | O SN_MCLK | O | | |
| S_GPI[25] | SN_PXCLK | SN_PXCLK | I | SN_PXCLK | I | | |
| S_GPI[26] | SN_VD | SN_VD | I/O | SN_VD | I/O | | |
| S_GPI[27] | SN_HD | SN_HD | I/O | SN_HD | I/O | | |
| SN_DGPIO4 | | | | | CCIR_CLK | I CCIR_CLK | I |

Memory Card interface (29)

| Pin No. | Name | Type | Reset | Descriptions |
|---------|---------------------|------------|-------|--|
| L16 | SD_CAP | P | - | Internal Supply Voltage decoupling for SDIO interface. (3.3/1.8V switchable, default 3.3V) |
| W3 | MC0 C_GPIO[0] | / mvl/O | I p/u | Memory Card interface(see below table) |
| V4 | MC1 C_GPIO[1] | / mvl/O | I p/u | |
| U4 | MC2 C_GPIO[2] | / mvl/O | I p/u | |
| W4 | MC3 C_GPIO[3] | / mvl/O | I p/u | |
| U6 | MC4 C_GPIO[4] | / mvl/O | I p/u | |
| T4 | MC5 C_GPIO[5] | / mvl/O | I p/u | |
| W5 | MC6 C_GPIO[6] | / mvl/O | I p/u | |
| V6 | MC7 C_GPIO[7] | / mvl/O | I p/u | |
| T7 | MC8 C_GPIO[8] | / mvl/O | I p/u | |
| U5 | MC9 C_GPIO[9] | / mvl/O | I p/u | |
| V5 | MC10 C_GPIO[10] | / mvl/O | I p/u | |
| W6 | MC11 C_GPIO[11] | / mvl/O | I p/u | |
| V7 | MC12 C_GPIO[12] | / mvl/O | I p/d | |
| T8 | MC13 C_GPIO[13] | / mvl/O | I p/d | |
| W7 | MC14 C_GPIO[14] | / mvl/O | I p/u | |
| U7 | MC15 C_GPIO[15]* | / mvl/O | I p/u | |
| M19 | MC16 C_GPIO[16] | / I/Os | I p/d | |
| M18 | MC17 C_GPIO[17] | / I/O | I p/u | |
| M17 | MC18 C_GPIO[18] | / I/O | I p/u | |
| M16 | MC19 C_GPIO[19] | / I/O | I p/u | |
| N19 | MC20 C_GPIO[20] | / I/O | I p/u | |

| | | | | |
|-----|---------------------|---|------|-------|
| N18 | MC21 C_GPIO[21]* | / | I/O | I p/u |
| N16 | MC22 C_GPIO[22]* | / | I/Os | I p/d |
| N17 | MC23 C_GPIO[23]* | / | I/O | I p/u |
| N13 | MC24 C_GPIO[24]* | / | I/O | I p/u |
| P13 | MC25 C_GPIO[25]* | / | I/O | I p/u |
| M13 | MC26 C_GPIO[26]* | / | I/O | I p/u |
| M14 | MC27 C_GPIO[27]* | / | I/O | I p/u |

Note*: The pin can trigger interrupt.

Note1: The mvI/O voltage of MC0~15 corresponds to VDD_MC.

Note2: The IO voltage of MC16~21 corresponds to SD_CAP, it could be switched between 3.3/1.8V by the register.

Memory card interface pinmux table

| Name | NAND Flash | SD/MMC/eMMC | SD | SPI flash | I2S | | | |
|------|------------|-------------|----------|-----------|-------------|-----|----------|-----|
| MC0 | NAND_D0 | I/O | eMMC_D0 | I/O | SPI_DO/D0 | I/O | | |
| MC1 | NAND_D1 | I/O | eMMC_D1 | I/O | SPI_DI/D1 | I/O | | |
| MC2 | NAND_D2 | I/O | eMMC_D2 | I/O | SPI_CLK | O | | |
| MC3 | NAND_D3 | I/O | eMMC_D3 | I/O | SPI_WP/D2 | I/O | | |
| MC4 | NAND_D4 | I/O | eMMC_D4 | I/O | SPI_HOLD/D3 | I/O | | |
| MC5 | NAND_D5 | I/O | eMMC_D5 | I/O | | | | |
| MC6 | NAND_D6 | I/O | eMMC_D6 | I/O | | | | |
| MC7 | NAND_D7 | I/O | eMMC_D7 | I/O | | | | |
| MC8 | NAND_CS0# | O | | | SPI_CS# | O | | |
| MC9 | NAND_CS1# | O | eMMC_CLK | O | | | | |
| MC10 | NAND_WE# | O | | | | | | |
| MC11 | NAND_RE# | O | eMMC_CMD | I/O | | | | |
| MC12 | NAND_CLE | O | | | | | | |
| MC13 | NAND_ALE | O | | | | | | |
| MC14 | NAND_WP# | O | | | | | | |
| MC15 | NAND_RDY | I | | | | | | |
| MC16 | | | SD_CLK | O | | | | |
| MC17 | | | SD_CMD | I/O | | | | |
| MC18 | | | SD_D0 | I/O | | | | |
| MC19 | | | SD_D1 | I/O | | | | |
| MC20 | | | SD_D2 | I/O | | | | |
| MC21 | | | SD_D3 | I/O | | | | |
| MC22 | | SDIO_CLK | O | | SPI_CLK | O | I2S_MCLK | O |
| MC23 | | SDIO_CMD | I/O | | SPI_CS# | O | I2S_BCLK | I/O |
| MC24 | | SDIO_D0 | I/O | | SPI_DI | I | I2S_SYNC | O |
| MC25 | | SDIO_D1 | I/O | | SPI_DO | O | I2S_DO | O |
| MC26 | | SDIO_D2 | I/O | | | | I2S_DI | I |
| MC27 | | SDIO_D3 | I/O | | | | | |

LCD interface (23)

| Pin No. | Name | Type | Reset | Descriptions |
|---------|------|------|-------|--------------|
|---------|------|------|-------|--------------|

| | | | | | |
|-----|----------------------------|---|-------|-------|---|
| T11 | LCD0 L_GPIO[0] BS0 | / | mvl/O | I p/d | LCD Signal Bus / BS2..0 : BOOT_SRC The boot source setting description: 0x0: NAND with RS ECC |
| U11 | LCD1 L_GPIO[1] BS1 | / | mvl/O | I p/d | 0x1: Boot card (Select by BOOT_CARD) 0x2: eMMC (SDIO2_2) 0x3: USB full speed |
| W10 | LCD2 L_GPIO[2] BS2 | / | mvl/O | I p/d | 0x4: SPI flash 0x5: USB high speed 0x6: NAND with Hamming ECC 0x7: BMC (SPI) |
| V10 | LCD3 L_GPIO[3] BS3 | / | mvl/O | I p/d | LCD Signal Bus / BS3 : Reserved for F/W(MPLL control flow) BS6..3 is for IC debugging setting. Please keep low at reset signal rising edge. |
| U10 | LCD4 L_GPIO[4] BS4 | / | mvl/O | I p/d | LCD Signal Bus / BS4 : BOOT_CARD Boot card select 0: SDIO 1: SDIO2 (SDIO2_2) |
| T10 | LCD5 L_GPIO[5] BS5 | / | mvl/O | I p/d | LCD Signal Bus / BS5 : EJTAG_SEL EJTAG select 0: GPIO (TRST, TMS, TCK, TDI, TDO are GPIO) 1: EJTAG |
| W9 | LCD6 L_GPIO[6] BS6 | / | mvl/O | I p/d | LCD Signal Bus / BS6 : MPLL_CLK_SEL Select clock source of PLL. 0: APLL clock output (From APLL clock) 1: Bypass APLL (From external clock) |
| V9 | LCD7 L_GPIO[7] BS7 | / | mvl/O | I p/d | LCD Signal Bus / BS7 : EMMC_BUSWIDTH eMMC boot bus width 0: 4 bits data bus 1: 8 bits data bus |
| U9 | LCD8 L_GPIO[8] | / | mvl/O | I p/d | LCD Signal Bus |
| T9 | LCD9 L_GPIO[9] | / | mvl/O | I p/d | |
| W8 | LCD10 L_GPIO[10] | / | mvl/O | I p/d | |
| V8 | LCD11 L_GPIO[11] | / | mvl/O | I p/d | |
| U8 | LCD12 L_GPIO[12] BS8 | / | mvl/O | I p/d | LCD Signal Bus / BS8 : EMMC_BOOTMODE eMMC boot mode 0: single rate + backward timing 1: dual rate + high speed timing |
| N11 | LCD13 L_GPIO[13] BS9 | / | mvl/O | I p/d | LCD Signal Bus/ BS9 : EMMC_DDR_DATA_ORDER eMMC DDR data order 0: Odd byte (1 st byte) first 1: Even byte (2 nd byte) first |
| M11 | LCD14 | / | mvl/O | I p/d | LCD Signal Bus/ BS10 : MIPS_DEBUG_MODE_SEL |

| | | | | | |
|-----|----------------------|---|-------|-------|--|
| | L_GPIO[14] BS10 | / | | | Enable NT96650 enters CPU debug mode. Internal CPU state will be outputted to debug port on storage interface (MC[18..0]) 0: Normal mode 1: CPU debug mode BS10 for IC debugging setting. Please keep low at reset signal rising edge. |
| M11 | LCD14 L_GPIO[14] | / | mvl/O | I p/d | LCD Signal Bus |
| N10 | LCD15/ L_GPIO[15] | / | mvl/O | I p/d | |
| M10 | LCD16 L_GPIO[16] | / | mvl/O | I p/d | |
| P7 | LCD17 L_GPIO[17] | / | mvl/O | I p/d | |
| N6 | LCD18 L_GPIO[18]* | / | mvl/O | I p/d | |
| M7 | LCD19 L_GPIO[19]* | / | mvl/O | I p/d | |
| M6 | LCD20 L_GPIO[20] | / | mvl/O | I p/d | |
| N7 | LCD21 L_GPIO[21] | / | mvl/O | I p/d | |
| P6 | LCD22 L_GPIO[22] | / | mvl/O | I p/d | |

Note1: The mvl/O voltage of LCD interface corresponds to VDD_LCD.

LCD interface pinmux table

| Name | CCIR(8 bits) | | Serial RGB | | CCIR(16 bits) | | i80/M68 | | CCIR & RGB (secondary panel) | | MPU Serial (secondary panel) | |
|-------|--------------|---|------------|---|---------------|---|---------|-----|---------------------------------|---|---------------------------------|-----|
| LCD0 | CCIR_YC0 | O | RGB_D0 | O | CCIR_Y0 | O | MPU_D0 | I/O | | | | |
| LCD1 | CCIR_YC1 | O | RGB_D1 | O | CCIR_Y1 | O | MPU_D1 | I/O | | | | |
| LCD2 | CCIR_YC2 | O | RGB_D2 | O | CCIR_Y2 | O | MPU_D2 | I/O | | | | |
| LCD3 | CCIR_YC3 | O | RGB_D3 | O | CCIR_Y3 | O | MPU_D3 | I/O | | | | |
| LCD4 | CCIR_YC4 | O | RGB_D4 | O | CCIR_Y4 | O | MPU_D4 | I/O | | | | |
| LCD5 | CCIR_YC5 | O | RGB_D5 | O | CCIR_Y5 | O | MPU_D5 | I/O | | | | |
| LCD6 | CCIR_YC6 | O | RGB_D6 | O | CCIR_Y6 | O | MPU_D6 | I/O | | | | |
| LCD7 | CCIR_YC7 | O | RGB_D7 | O | CCIR_Y7 | O | MPU_D7 | I/O | | | | |
| LCD8 | CCIR_CLK | O | RGB_CLK | O | CCIR_CLK | O | MPU_TE | I | | | | |
| LCD9 | CCIR_VD | O | RGB_VD | O | CCIR_VD | O | MPU_CS# | O | | | | |
| LCD10 | CCIR_HD | O | RGB_HD | O | CCIR_HD | O | MPU_RS | O | | | | |
| LCD11 | | | | | CCIR_DE | O | MPU_WR# | O | | | | |
| LCD12 | | | | | CCIR_C0 | O | MPU_RD# | O | RGB_YC0 | O | | |
| LCD13 | | | | | CCIR_C1 | O | MPU_D8 | I/O | RGB_YC1 | O | MPU_SDO | O |
| LCD14 | | | | | CCIR_C2 | O | MPU_D9 | I/O | RGB_YC2 | O | MPU_SDI | I |
| LCD15 | | | | | CCIR_C3 | O | MPU_D10 | I/O | RGB_YC3 | O | MPU_CS | O |
| LCD16 | | | | | CCIR_C4 | O | MPU_D11 | I/O | RGB_YC4 | O | MPU_RS | O |
| LCD17 | | | | | CCIR_C5 | O | MPU_D12 | I/O | RGB_YC5 | O | MPU_CLK | O |
| LCD18 | | | | | CCIR_C6 | O | MPU_D13 | I/O | RGB_YC6 | O | MPU_SDIO | I/O |
| LCD19 | | | | | CCIR_C7 | O | MPU_D14 | I/O | RGB_YC7 | O | MI_TE | I |
| LCD20 | LCD_CS | O | | | | | MPU_D15 | I/O | RGB_CLK | O | | |
| LCD21 | LCD_CLK | O | | | | | MPU_D16 | I/O | RGB_VD | O | | |
| LCD22 | LCD_DAT | O | | | | | MPU_D17 | I/O | RGB_HD | O | | |

PWM (20)

| Pin No. | Name | Type | Reset | Descriptions |
|---------|---------------------------------|------|-------|--------------|
| B3 | PWM0 ME_SHUT0 P_GPIO[36] | / | I/O | I p/d |
| C3 | PWM1 ME_SHUT1 P_GPIO[37] | / | I/O | I p/d |
| D4 | PWM2 P_GPIO[38] | / | I/O | I p/d |
| D3 | PWM3 P_GPIO[39] | / | I/O | I p/d |
| E3 | PWM4 P_GPIO[40] | / | I/O | I p/d |
| G7 | PWM5 P_GPIO[41] | / | I/O | I p/d |
| F7 | PWM6 P_GPIO[42] | / | I/O | I p/d |
| L6 | PWM7 P_GPIO[43] | / | I/O | I p/d |
| J6 | PWM8 P_GPIO[44] | / | I/O | I p/d |
| K6 | PWM9 P_GPIO[45] | / | I/O | I p/d |
| K7 | PWM10 P_GPIO[46] | / | I/O | I p/d |
| L7 | PWM11 P_GPIO[47] | / | I/O | I p/d |
| C17 | PWM12 P_GPIO[48] | / | I/O | I p/d |
| D16 | PWM13 P_GPIO[49] | / | I/O | I p/d |
| C15 | PWM14 P_GPIO[50] | / | I/O | I p/d |
| B17 | PWM15 P_GPIO[51] | / | I/O | I p/d |
| G13 | PWM16 ME_SHUT0 P_GPIO[52] | / | I/O | I p/d |
| H14 | PWM17 ME_SHUT1 P_GPIO[53] | / | I/O | I p/d |
| J13 | PWM18 P_GPIO[54]* | / | I/O | I p/d |
| G14 | PWM19 P_GPIO[55]* | / | I/O | I p/d |

| Name | PWM | | M-shutter | | u-stepping | | SPI | | | | |
|-------|-------|---|-----------|---|------------|---|----------|---|--|--|--|
| PWM0 | PWM0 | O | ME_SHUT0 | O | uSTP1_A | O | | | | | |
| PWM1 | PWM1 | O | ME_SHUT1 | O | uSTP1_B | O | | | | | |
| PWM2 | PWM2 | O | | | uSTP1_C | O | | | | | |
| PWM3 | PWM3 | O | | | uSTP1_D | O | | | | | |
| PWM4 | PWM4 | O | | | uSTP2_A | O | SPI3_CLK | O | | | |
| PWM5 | PWM5 | O | | | uSTP2_B | O | SPI3_CS# | O | | | |
| PWM6 | PWM6 | O | | | uSTP2_C | O | SPI3_DO | O | | | |
| PWM7 | PWM7 | O | | | uSTP2_D | O | SPI3_DI | O | | | |
| PWM8 | PWM8 | O | | | uSTP3_A | O | | | | | |
| PWM9 | PWM9 | O | | | uSTP3_B | O | | | | | |
| PWM10 | PWM10 | O | | | uSTP3_C | O | | | | | |
| PWM11 | PWM11 | O | | | uSTP3_D | O | | | | | |
| PWM12 | PWM12 | O | | | uSTP4_A | O | | | | | |
| PWM13 | PWM13 | O | | | uSTP4_B | O | | | | | |
| PWM14 | PWM14 | O | | | uSTP4_C | O | | | | | |
| PWM15 | PWM15 | O | | | uSTP4_D | O | | | | | |
| PWM16 | PWM16 | O | ME_SHUT0 | O | | | | | | | |
| PWM17 | PWM17 | O | ME_SHUT1 | O | | | | | | | |
| PWM18 | PWM18 | O | | | | | | | | | |
| PWM19 | PWM19 | O | | | | | | | | | |

Peripheral I/O (19)

| Pin No. | Name | Type | Reset | Descriptions |
|---------|-------------------------------------|--------|-------|--|
| E19 | I2C_SDA P_GPIO[0]* | / I/OD | I p/u | I2C-BUS clock output(Open Drain IO structure) |
| F17 | I2C_SCL P_GPIO[1]* | / I/OD | I p/u | I2C-BUS data input / output(Open Drain IO structure) |
| C19 | SB_CS2 SPI3_CS P_GPIO[7]* | / I/O | I p/u | Serial Interface Chip Select 2 Serial Peripheral Interface 3 chip select output |
| C18 | SB_CS3 SPI3_DI P_GPIO[8]* | / I/O | I p/u | Serial Interface Chip Select 3 Serial Peripheral Interface 3 data input |
| B19 | SB_CK23 SPI3_CLK P_GPIO[9]* | / I/O | I p/d | Serial Interface Clock 2 & 3 Serial Peripheral Interface 3 clock output |
| A19 | SB_DAT23 SPI3_DO P_GPIO[10]* | / I/O | I p/d | Serial Interface Data 2 & 3 Serial Peripheral Interface 3 data output |
| A17 | UART_TX P_GPIO[15] | / I/O | O | UART Transmit |
| B16 | UART_RX P_GPIO[16]* | / I/O | I p/u | UART Receive |
| J14 | UART2_TX SPI2_CS P_GPIO[17]* | / I/O | I p/u | UART2 Transmit Serial Peripheral Interface 2 chip select output |
| F13 | UART2_RX SPI2_CLK P_GPIO[18]* | / I/O | I p/u | UART2 Receive Serial Peripheral Interface 2 clock output |

| | | | | | |
|-----|-------------------------------------|---|-------|-------|--|
| H13 | UART2_RTS SPI2_DO P_GPIO[19]* | / | I/O | I p/u | UART2 Request To Send Serial Peripheral Interface 2 data output |
| A18 | UART2_CTS SPI2_DI P_GPIO[20]* | / | I/O | I p/u | UART2 Clear To Send Serial Peripheral Interface 2 data input |
| B18 | REMOTE_RX PICNT3 P_GPIO[25]* | / | I/Oss | I p/u | Infrared Remote-control Received Data Pulse Counter 3 input |
| A3 | FL_TRIG S_GPIO[28] | / | I/O | I p/d | Flash Light Trigger Control |
| F6 | SP_CLK PICNT4 S_GPIO[29]* | / | I/Oss | I p/d | Clock Output for Micro-stepping Motor Control Pulse Counter 4 input |
| A16 | PICNT1 DGPI00* | / | I/Osw | I p/d | Pulse Counter 1 input |
| C16 | PICNT2 DGPI01* | / | I/Osw | I p/d | Pulse Counter 2 input |
| C13 | SD_CD# DGPI02* | / | I/Osw | I p/u | Card Detect input pin |
| A15 | SD_WP# DGPI03* | / | I/Osw | I p/u | Write protect input pin |

ADC interface (8)

| Pin No. | Name | Type | Reset | Descriptions |
|---------|---------|------|-------|--|
| U12 | AD_IN0 | AI | - | General ADC 0 Input with buffer. |
| T13 | AD_IN1* | AI | - | General ADC 1 Input with configurable trigger function |
| W14 | AD_IN2* | AI | - | General ADC 2 Input with configurable trigger function |
| T12 | AD_IN3 | AI | - | General ADC 3 Input with buffer. |
| V14 | AD_INX | AI | - | General ADC X Input and Touch Panel Control Interface |
| U14 | AD_INY | AI | - | General ADC Y Input and Touch Panel Control Interface |
| W15 | TP_YP | AI | - | Touch Panel Control Interface |
| V15 | TP_XM | AI | - | Touch Panel Control Interface |

Audio Codec(10)

| Pin No. | Name | Type | Reset | Descriptions |
|---------|----------|------|-------|--|
| W19 | MIC_BIAS | AO | - | Microphone working bias output. |
| U19 | MIC_RINP | AI | - | Right channel microphone differential input positive side. |
| U18 | MIC_RINN | AI | - | Right channel microphone differential input negative side. |
| V19 | MIC_LINP | AI | - | Left channel microphone differential input positive side. |
| V18 | MIC_LINN | AI | - | Left channel microphone differential input negative side. |
| U17 | VMIDX | AO | - | Decoupling for audio codec reference voltage. Connect 4.7uF capacitor to ground. |
| W16 | HP_R | AO | - | Right channel headphone output. (or Line out) |
| V16 | HP_L | AO | - | Left channel headphone output. (or Line out) |
| W17 | SPK_P | AO | - | Speaker Output of Right Channel |

| | | | | |
|-----|-------|----|---|--------------------------------|
| W18 | SPK_N | AO | - | Speaker Output of Left Channel |
|-----|-------|----|---|--------------------------------|

TV interface (2)

| Pin No. | Name | Type | Reset | Descriptions |
|---------|----------|------|-------|--|
| J17 | TV_CVBS | AO | - | Video Data Output Composite video output. |
| K17 | TV_FSADJ | AI | - | Full Screen Adjust Pin TV DAC Full-scale adjust control pin. A 470 Ω /1% resistor connected between this pin and GND controls the full-scale output current on the TV_CVBS output. |

MIPI DSI (7)

| Pin No. | Name | Type | Reset | Descriptions |
|---------|---------|------|-------|---|
| P11 | DSI_CAP | P | - | Internal Supply Voltage decoupling for DSI LP mode circuit. |
| V12 | DSI_CKP | AO | - | MIPI DSI differential clock lane output |
| W12 | DSI_CKN | AO | - | |
| V11 | DSI_D0P | AO | - | MIPI DSI differential data lane input / output |
| W11 | DSI_D0N | AO | - | |
| V13 | DSI_D1P | AO | - | |
| W13 | DSI_D1N | AO | - | |

HDMI (13)

| Pin No. | Name | Type | Reset | Descriptions |
|---------|--------------------------|---------------------|-------|--|
| L18 | HDMI_TXCP | AO | - | TMDS Low Voltage Differential Signal Output Clock |
| L19 | HDMI_TXCN | | | |
| K18 | HDMI_TX0P | AO | - | TMDS Low Voltage Differential Signal Output Data |
| K19 | HDMI_TX0N | | | |
| J18 | HDMI_TX1P | | | |
| J19 | HDMI_TX1N | | | |
| H18 | HDMI_TX2P | | | |
| H19 | HDMI_TX2N | | | |
| H16 | HDMI_REXT | AI | - | Voltage Swing Adjust. Connect 1.2K Ω /1% resistor to HDMI GND |
| E18 | HDMI_CEC P_GPIO[27]* | I/O _{5VT} | I p/u | Consumer Electronics Control. CEC is 5V tolerance input. |
| D18 | DDC_SDA P_GPIO[28] | I/OD _{5VT} | I p/u | Display Data Channel SDA. DDCSDA is 5V tolerance input. |
| D19 | DDC_SCL P_GPIO[29] | I/OD _{5VT} | I p/u | Display Data Channel SCL. DDCSCL is 5V tolerance input. |
| E17 | HDMI_PLUG P_GPIO[30]* | I/O _{5VT} | I p/d | Hot Plug Detect. HOTPLUG is 5V tolerance input. |

USB device interface (4)

| Pin No. | Name | Type | Reset | Descriptions |
|---------|----------|-------------------|-------|--|
| D17 | VBUSI* | I _{5VTZ} | I p/d | USB V _{BUS} Input. This pin is 5V tolerance input |
| F19 | USB_DP | AI/O | - | USB FS/HS Differential Data Plus (D+) |
| G19 | USB_DM | AI/O | - | USB FS/HS Differential Data Minus (D-) |
| G18 | USB_RREF | AI | - | USB reference resistor. Connect 12KΩ/1% resistor to GND |

Power (73)

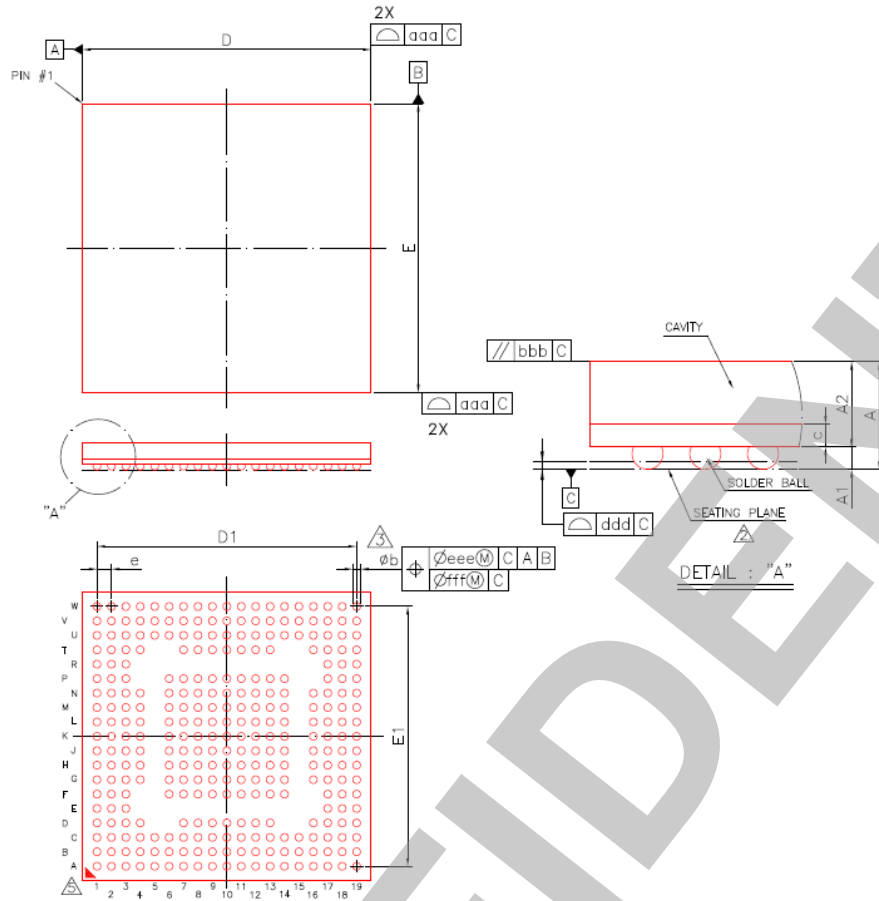
| Pin No. | Name | Type | Descriptions |
|--|-------------|------|---|
| F12, G12, H6, H7, J7, K13, L13, L14, N8, N9, P8 | VDDK(11) | P | Core Power |
| F14, G6, P14 | VDD_IO(3) | P | I/O Pad Power |
| H9, H10, H11, J8, J9, J10, J11, K8, K9, K10, K11, K12, L8, L9, L10, L11, L12, M8, M9 | GND(19) | P | Digital Ground |
| F3, H4, L4, G4, K4, J3 | VDD_DR(6) | P | DRAM I/O power. (1.8V for DDRII; 1.5V for DDRIII.) |
| H3 | AVDD_DR_1V | P | Analog 1.0V power for DDR PHY |
| G3 | AVDD_DLL(1) | P | DLL power. (3.3V power for HV version, 1.5/1.8V for LV version) |
| K3 | AGND_DLL(1) | P | Ground for DLL |
| G11 | VDD_RTC(1) | P | RTC Power |
| F11 | VDD_VBAT(1) | P | Battery input for power button controller |
| V3 | VDD_MC(1) | P | Multi-level IO power for Memory Card |
| F8, G9 | AVDD_HSI_K | P | Analog 1.0V power for HSI core power |
| F9 | AVDD_HSI_RX | P | Analog 3.3V power for HSI receiver |
| F10 | VDD_HSI_IO | P | Multi-level input power of HSI |
| G10, H8 | AGND_HSI(2) | P | Ground for High Speed Interface |
| G8 | VDD_SN | P | Multi-level IO Power for sensor interface |
| P9, P10 | VDD_LCD(2) | P | Multi-level IO power for LCD interface |
| L17 | VDD_SDLI | P | LDO's input power for Card IO |
| P12 | AVDD_DSI_K | P | Analog power for MIPI DSI core |
| N12 | VDD_DSI_IO | P | LDO's input power for MIPI DSI LP IO |
| M12 | AGND_DSI | P | Ground for MIPI DSI |
| U13 | AVDD_ADC | P | Analog 3.3V power for ADC |
| U15 | AGND_ADC | P | Ground for ADC |
| K16 | AVDD_DAC | P | Analog 3.3V power for TV DAC |
| J16 | AGND_DAC | P | Ground for TV DAC |
| T17 | AVDD_AUD | P | Analog 3.3V power for Audio Codec |
| V17 | AGND_AUD | P | Ground for Audio Codec |
| T16 | AVDD_SPK | P | Analog 3.3V power for Speaker Amplifier |

| | | | |
|-----|-------------|---|----------------------------------|
| U16 | AGND_SPK | P | Ground for Speaker Amplifier |
| K14 | AVDD_HDMI | P | Analog HDMI interface Power |
| H17 | AGND_HDMI | P | Ground for HDMI interface |
| G16 | AVDD_USB_LI | P | LDO's input power for USB PHY |
| F18 | VDD_USB_FS | P | USB Full Speed Transceiver Power |
| G17 | AGND_USB | P | Ground for USB |
| T19 | AVDD_MPLL | P | Multiple PLL analog Power |
| T18 | AGND_MPLL | P | PLL analog Power |

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Package Outline

TFBGA-305



| Symbol | Dimension In mm | | | Dimension In Inch | | |
|--------|-----------------|-------|-------|-------------------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | --- | --- | 1.30 | --- | --- | 0.051 |
| A1 | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| A2 | 0.91 | 0.96 | 1.01 | 0.036 | 0.038 | 0.040 |
| c | 0.22 | 0.26 | 0.30 | 0.009 | 0.010 | 0.012 |
| D | 12.90 | 13.00 | 13.10 | 0.508 | 0.512 | 0.516 |
| E | 12.90 | 13.00 | 13.10 | 0.508 | 0.512 | 0.516 |
| D1 | --- | 11.70 | --- | --- | 0.461 | --- |
| E1 | --- | 11.70 | --- | --- | 0.461 | --- |
| e | --- | 0.65 | --- | --- | 0.026 | --- |
| b | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| aaa | --- | 0.15 | --- | --- | 0.006 | --- |
| bbb | --- | 0.10 | --- | --- | 0.004 | --- |
| ddd | --- | 0.10 | --- | --- | 0.004 | --- |
| eee | --- | 0.15 | --- | --- | 0.006 | --- |
| fff | --- | 0.08 | --- | --- | 0.003 | --- |
| MD/ME | --- | 19/19 | --- | --- | 19/19 | --- |

- NOTE :
- CONTROLLING DIMENSION : MILLIMETER.
 - PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
 - DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
 - SPECIAL CHARACTERISTICS C CLASS: bbb, ddd
 - THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
 - REFERENCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5

Electrical Characteristics

Absolute Maximum Ratings

| Item | Symbol | Rating | Unit |
|---|--|---------------------------|-------------|
| Supply Voltage of 1.0V Core power | V_{DDK} | -0.3 ~ +1.2 | V |
| Supply Voltage of DRAM I/O | V_{DD_DR} | -0.3 ~ +2.1 | V |
| Supply Voltage of 3.3V Digital I/O | $V_{DD_IO}, V_{DD_RTC},$ $V_{DD_VBAT}, V_{DD_SDLI},$ $V_{DD_DSI_IO}$ | -0.3 ~ +3.8 | V |
| Supply Voltage of multi-level I/O | $V_{DD_MC}, V_{DD_HSL_IO},$ V_{DD_SN}, V_{DD_LCD} | -0.3 ~ +3.8 | V |
| Supply Voltage of 1.0V analog block | $AV_{DD_DR_1V},$ $AV_{DD_HSL_K},$ $AV_{DD_DSI_K},$ AV_{DD_MPLL} | -0.3 ~ +1.2 | V |
| Supply Voltage of 1.5/1.8V analog block | $*AV_{DD_DLL},$ $AV_{DD_HDMI},$ $AV_{DD_USB_LI}$ | -0.3 ~ +2.1 | V |
| Supply Voltage of 3.3V analog block | $*AV_{DD_DLL},$ $AV_{DD_HSL_RX},$ $AV_{DD_USB_FS},$ $AV_{DD_ADC},$ $AV_{DD_DAC},$ $AV_{DD_AUD},$ $AV_{DD_SPK},$ | -0.3 ~ +3.8 | V |
| Input/Output Voltage | I/O | -0.3 ~ $V_{DD_IO} + 0.3$ | V |
| Input Voltage(5V Tolerant) | I/O_{5VT} | -0.3 ~ +5.8 | V |
| Operating Ambient Temperature | T_{OPR} | -10 ~ 70 | $^{\circ}C$ |
| Storage Temperature | T_{STG} | -55 ~ 125 | $^{\circ}C$ |

* AV_{DD_DLL} : Supply 3.3V for HV version, 1.5/1.8V for LV version

Comment

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

ESD performance

| Model | Standard | Classification | Note |
|----------------------|-------------------------------------|----------------|----------|
| Human Body Mode(HBM) | MIL-STD-883G Method 3015.7 | Class : 2 | 2K~3KV |
| Machine Mode(MM) | JEDEC Specification EIA/JESD22-A115 | Class : B | 200~400V |
| CDM Mode(CDM) | JEDEC Specification JESD22-C101 | | |

Latch-up Immunity

| Model | Standard | Classification | Note |
|----------|------------------------------|----------------|--------|
| Latch up | JEDEC Specification JESD-78A | Class : I | ±200mA |

Recommended Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|------------------------|--|-------|------|-------|------|-------------|
| V _{DDK} | Core Logic Operating Voltage | 0.9 | 1.0 | 1.1 | V | |
| V _{DD_DR} | DDRII DRAM Interface Operating Voltage | 1.7 | 1.8 | 1.9 | V | DDRII DRAM |
| V _{DD_DR} | DDRIII DRAM Interface Operating Voltage | 1.425 | 1.5 | 1.575 | V | DDRIII DRAM |
| V _{DD_IO} | General I/O Interface Operating Voltage | 3.0 | 3.3 | 3.6 | V | |
| V _{DD_RTC} | RTC Operating Voltage | 1.5 | - | 3.6 | V | |
| V _{DD_RTC} | RTC Maintenance Voltage | 1 | - | 3.6 | V | |
| V _{DD_VBAT} | Power Controller Operating Voltage | 1.5 | - | 3.6 | V | |
| V _{DD_SDLI} | I/O of SD Card Operating Voltage | 3.0 | 3.3 | 3.6 | V | |
| V _{DD_DSI_IO} | LDO of MIPI DSI Operating Voltage | 3.0 | 3.3 | 3.6 | V | |
| V _{DD_MC} | I/O of Memory Card Interface Operating Voltage | 1.62 | 3.3 | 3.6 | V | 1.8V~3.3V |
| V _{DD_HSI_IO} | Input of High Speed Interface Operating Voltage | 1.62 | 3.3 | 3.6 | V | 1.8V~3.3V |
| V _{DD_SN} | I/O of Sensor Interface Operating Voltage | 1.62 | 3.3 | 3.6 | V | 1.8V~3.3V |
| V _{DD_LCD} | I/O of LCD Interface Operating Voltage | 1.62 | 3.3 | 3.6 | V | 1.8V~3.3V |
| AV _{DD_DR_1V} | Core Logic of DDR PHY Operating Voltage | 0.9 | 1.0 | 1.1 | V | |
| AV _{DD_HSI_K} | Core Logic of High Speed Interface Operating Voltage | 0.9 | 1.0 | 1.1 | V | |
| AV _{DD_DSI_K} | Core Logic of MIPI DSI Operating Voltage | 0.9 | 1.0 | 1.1 | V | |
| AV _{DD_MPLL} | MPLL Operating Voltage | 0.9 | 1.0 | 1.1 | V | |
| AV _{DD_DLL} | DLL Operating Voltage | 3.0 | 3.3 | 3.6 | V | HV version |
| AV _{DD_DLL} | DLL Operating Voltage | 1.425 | 1.5 | 1.9 | V | LV version |
| AV _{DD_HDMI} | Transceiver of HDMI | 1.425 | 1.5 | 1.9 | V | |

| | | | | | | |
|-------------------------|--|-------|-----|-----|---|--|
| | Operating Voltage | | | | | |
| AV _{DD_USB_LI} | LDO of USB PHY Operating Voltage | 1.425 | 1.5 | 1.9 | V | |
| AV _{DD_HSI_RX} | Receiver of High Speed Interface Operating Voltage | 3.0 | 3.3 | 3.6 | V | |
| AV _{DD_USB_FS} | Transceiver of USB Full Speed Operating Voltage | 3.0 | 3.3 | 3.6 | V | |
| AV _{DD_ADC} | ADC Operating Voltage | 3.0 | 3.3 | 3.6 | V | |
| AV _{DD_DAC} | Video DAC Operating Voltage | 3.0 | 3.3 | 3.6 | V | |
| AV _{DD_AUD} | Audio Codec Operating Voltage | 3.0 | 3.3 | 3.6 | V | |
| AV _{DD_SPK} | Speaker Amplifier Operating Voltage | 3.0 | 3.3 | 3.6 | V | |

AC/DC Characteristics

TBD

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